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10/729,701	12/05/2003	You-Pang Wei	033994-006	4588

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BUCHANAN, INGERSOLL & ROONEY PC
POST OFFICE BOX 1404
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EXAMINER	
JACOB, MARY C	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 11/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,701	WEI ET AL.	
	Examiner	Art Unit	
	Mary C. Jacob	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *13-22 and 33-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 23-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-36* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/3/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-36 have been presented for examination.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-12, 23-32, drawn to a method of simulating a memory circuit design in order to verify the signal strength of bit lines against a noise margin, classified in class 703, subclass 14.

II. Claims 13-22, drawn to a method of characterizing and determining a valid minimum clock cycle time, classified in class 703, subclass 19.

III. Claims 33-36, drawn to optimizing a circuit parameter, classified in class 716, subclass 2.

3. The inventions are independent or distinct, each from the other because:

Inventions I, II and III are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different designs, modes of operation, and effects (MPEP § 802.01 and § 806.06). In the instant case, the different inventions are the simulation of the memory circuit to verify signal strength of bit lines, the characterization and determination of a minimum clock cycle time and the optimization of a circuit parameter.

Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required

because the inventions require a different field of search (see MPEP § 808.02), restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Mr. Claude Hamrick on 11/8/06 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-12, 23-32. Affirmation of this election must be made by applicant in replying to this Office action. Claims 13-22 and 33-36 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

5. The drawings are objected to because Figure 3 is not discussed in the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the

examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

6. The disclosure is objected to because of the following informalities. Appropriate correction is required.

7. Page 2, line 2, "etc...." should be corrected to read, "etc."

8. Page 9, line 1 refers to step "201" in line 1 wherein it should refer to step "210".

Claim Objections

9. Claims 24 and 29 are objected to because of the following informalities. Appropriate correction is required.

10. Claim 24 recites "the sum" in lines 2-3, it would be better if written "a sum".

11. Claim 24 uses the word "and" in line 9, it would be better if written "or".

12. Claim 29 recites "the sum" in line 3, it would be better if written "a sum".

13. Claim 29 uses the word "and" in line 10, it would be better if written "or".

Claim Rejections - 35 USC § 112

14. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

15. Claims 1-12, 23-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

16. Claim 1 recites "the memory circuit" in line 5. It is unclear whether "the memory circuit" refers to the "memory circuit design" in line 3 or the "memory circuit path" that is extracted from circuit elements in line 4.

17. Claim 7 recites "the memory circuit" in line 6. It is unclear whether "the memory circuit" refers to the "memory circuit design" in line 4 or the "memory circuit path" that is extracted from circuit elements in line 5.

18. Claim 23 recites the limitation "the same status" in line 11. There is insufficient antecedent basis for this limitation in the claim.

19. Claim 23 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: what occurs if both simulations do not indicate the same status. The claim recites the final step of the method as follows, "ceasing simulation if both simulations indicate the same status", however, it fails to disclose what happens if both simulations do not indicate the same status, therefore, it is unclear what happens in this case.

20. Claim 24 recites the limitation "the current minimum value" in line 7. There is insufficient antecedent basis for this limitation in the claim.

21. Claim 24 recites the limitation "the current maximum value" in line 10. There is insufficient antecedent basis for this limitation in the claim.

22. Claim 27 recites the limitation "the measured noise" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

23. Claim 27 recites the limitation "the prescribed noise margin" in line 2. There is insufficient antecedent basis for this limitation in the claim.

24. Claim 28 recites the limitation "the same status" in line 12. There is insufficient antecedent basis for this limitation in the claim.

25. Claim 28 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: what occurs if both simulations do not indicate the same status. The claim recites the final step of the procedure executed by the computer as follows "halt operations if both simulations indicate the same status", however, it fails to disclose what happens if both simulations do not indicate the same status.

26. Claim 29 recites the limitation "the current minimum value" in line 8. There is insufficient antecedent basis for this limitation in the claim.

27. Claim 29, lines 8-12 both recite steps that include setting the current value of the parameter to the "current minimum value". It is unclear whether this is a correct limitation or whether the limitation in lines 11-12 should be directed to setting the current value of the parameter to the "current maximum" value.

28. Claim 32 recites the limitation "the prescribed noise margin" in line 2. There is insufficient antecedent basis for this limitation in the claim.

29. Due to the number of 35 U.S.C. 112, second paragraph rejections, the examiner has provided a number of examples of the claim deficiencies in the above rejection(s), however, the list of rejections may not be inclusive. Applicant should refer to these rejections as examples of deficiencies and should make all necessary corrections to eliminate the 35 U.S.C. 112, second paragraph problems and place the claims in proper format.

Due to the vagueness and a lack of a clear definition of the terminology and phrases used in the specification and claims, the claims have been treated on their merits as best understood by the examiner.

Claim Rejections - 35 USC § 101

30. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

31. Claims 1-12, 23-32 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims are a recitation of abstract ideas and fail to produce a concrete, useful or tangible result. For example, Claims 1 and 7 recite "comparing the maximum voltage difference between bit lines to a noise margin to verify the signal strength of the bit lines", however, this is a recitation of an abstract idea and even though the signal strength of the bit lines is "verified", there is no recitation of a concrete, useful or tangible result since there is no "real world" output of a result.

Claim Rejections - 35 USC § 103

32. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

33. Claims 1 and 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Laurent ("Sense Amplifier Signal Margins and Process Sensitivities", IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, Volume 49, No. 3, March 2002) view of Yuan et al (US Patent 6,249,901).

34. Laurent teaches: a method of simulating a memory circuit design in order to verify the signal strength of bit lines, the method comprising the steps of: simulating the memory circuit (section II, paragraph 1 and Figure 1); measuring a maximum voltage difference between bit lines (Figure 2; section II, paragraph 2); and comparing the

maximum voltage difference between bit lines to a noise margin to verify the signal strength of the bit lines (section II, paragraphs 3-5).

35. Laurent does not expressly teach identifying circuit elements of the memory circuit design and extracting a memory circuit path from the circuit elements.

36. Yuan et al teaches an automatic memory characterization system that provides improved accuracy in determining timing characteristics of a circuit (column 5, lines 64-67) wherein circuit elements of a memory circuit design are identified (Figure 5, elements 204, 208, 210; column 9, lines 35-39, lines 65-67), a memory circuit path is extracted from the circuit elements (Figure 5, elements 240 and 242; column 9, line 67-column 10, line 2; column 10, lines 45-52; Figure 8; column 19, lines 23-28) and the memory circuit is simulated (column 6, lines 54-56).

37. Laurent and Yuan et al are analogous art since they are both directed to the simulation and analysis of a memory circuit.

38. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of simulating a memory circuit design as taught in Laurent to further include identifying circuit elements of the memory circuit design and extracting a memory circuit path from the circuit elements as taught in Yuan et al since Yuan et al teaches an automatic memory characterization system that provides improved accuracy in determining timing characteristics of a circuit (column 5, lines 64-67).

39. Claims 2-6, 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laurent in view of Yuan et al as applied to claims 1 and 7 above, and further in view of Sandhu (US Patent 5,521,874).

40. Laurent in view of Yuan et al teach (claims 1 and 7) simulating a memory circuit design in order to verify the signal strength of bitlines, (claims 4 and 10) measuring the voltage difference between bit lines at a sensing time (Figure 2), and (claims 5 and 11) comparing the voltage difference between bit lines to a noise margin at the sensing time to verify the signal strength of the bit lines (section II, paragraphs 3-5).

41. Laurent in view of Yuan et al do not expressly teach (claims 2, 6, 8 and 12) wherein the voltage difference between bit lines is the voltage difference between bit and bitb lines and (claims 3 and 9) identifying sense amplifier enable node after extracting the memory circuit path.

42. Sandhu teaches a novel differential to single ended sense amplifier that utilizes a minimum number of stages to convert a differential input signal received from complementary bit lines to a single ended output signal indicative of the state of the data stored in a selected memory cell connected to the complementary bit lines wherein the circuit is constructed to operate with low voltage swings thereby increasing the switching speed and the sense speed (column 2, line 65-column 3, line 6). Sandhu teaches complementary bitlines, bit and bitb, that apply complementary signals to the input of a differential sense amplifier (column 1, lines 45-53) and a sense amplifier enable node that enables or disables the current sources in the circuit stages, thereby powering down the sense amplifier (column 5, lines 3-14).

43. Laurent in view of Yuan et al and Sandhu et al are analogous art since they are both directed to the design of a memory circuit that includes sense amplifiers.

44. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the simulating of a memory circuit design to verify the signal strength of bitlines as taught in Laurent and Yuan et al to further include the measurement of the voltage differential to be between the bit and bitb lines and by identifying the sense amplifier enable node since Sandhu teaches a novel differential to single ended sense amplifier that utilizes a minimum number of stages to convert a differential input signal received from complementary bit lines to a single ended output signal indicative of the state of the data stored in a selected memory cell connected to the complementary bit lines wherein the circuit is constructed to operate with low voltage swings thereby increasing the switching speed and this the sense speed (column 2, line 65-column 3, line 6) and further teaches that the inputs to a differential sense amplifier are the bit and bitb lines (column 1, lines 45-53) and that the sense amplifier enable signal enables the sense amplifier to operate (column 5, lines 3-14).

45. Claims 23-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yuan et al in view of Poon ("Computer Circuits Electrical Design", Prentice Hall, Inc., 1995, pages 63-69, 195-196, 220-221).

46. As to Claims 23 and 28, Yuan et al teaches: identifying circuit elements to be characterized (Figure 5, elements 204, 208, 210; column 9, lines 35-39, lines 65-67); extracting a critical path netlist from the circuit elements (Figure 5, elements 240 and

242; column 9, line 67-column 10, line 2; column 10, lines 45-52; Figure 8; column 19, lines 23-28); simulating the critical path netlist with a maximum initial value of the parameter under characterization (column 10, lines 50-52; Figure 11A, element 558); simulating the critical path netlist with a minimum initial value of the parameter under characterization (Figure 11A, element 562; column 21, lines 35-38; column 20, lines 19-22); calculating a criterion parameter (column 20, element 16-42; Figure 11A, elements 556, 558, 562; column 21, lines 17-21); determining whether the simulations based on the initial minimum and maximum values of the parameter under characterization indicate the same status (Figure 11A, element 566; column 21, element 52-56); and ceasing simulation if both simulations indicate the same status (column 20, lines 33-47).

47. As to Claims 24 and 29, Yuan et al teaches: determining a current value of the parameter under characterization that is half the sum of the maximum initial and minimum initial values of the parameter (column 22, equation 2); simulating the critical path netlist with the current value of the parameter and determining whether the simulation indicates a success or failed status (Figure 11A, elements 568-556; Figure 11B, elements 592, 594, 596); setting the current value of the parameter to the current minimum value of the parameter if both simulations based on the two values of the parameter indicate the same status (Figure 11B, elements 596 and 598); and setting the current value of the parameter to the current maximum value of the parameter otherwise (Figure 11B, elements 600-602).

48. As to Claims 25 and 30, Yuan et al teaches: determining a new current value of the parameter under characterization, simulating the critical path netlist with the new

value of the parameter and determining whether the simulations indicate a success or failed status until the criterion parameter converges to a prescribed bisection (prescribed value) (Figures 11A and 11B and descriptions, specifically, elements 570, 572, 574 and 576).

49. As to Claims 26 and 31, Yuan et al teaches: wherein the simulation indicates a success or failed status if a data output error of the simulation is above a prescribed threshold (column 20, lines 16-42; column 21, lines 29-51).

50. As to Claims 27 and 32, Yuan et al teaches: wherein the simulation indicates a failed status if the measured parameter is above a prescribed threshold (column 21, lines 28-51) wherein success and failure indicate opposite results in the optimization process.

51. Yuan et al does not expressly teach the characterizing a circuit parameter sensitive to a noise disturbance against a noise margin in a circuit design.

52. Poon teaches that device noise margin varies across device samples due to process variations and because of this, the range of the device noise margin must be taken into account in setting up circuit rules and careful attention must be paid to all aspects of noise analysis to maintain system reliability (page 64). Poon further teaches existing software that is used interactively for on-line feedback of layout decisions and allows for the analysis of a complete design to review the sources of nets that violate a user-defined noise margin (page 220, paragraph 3, "Valid Logic Systems...").

53. Yuan et al and Poon are analogous art since they are both directed to the design, simulation and analysis of an electrical circuit.

54. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of characterizing a circuit parameter as taught in Yuan et al to include characterizing the circuit parameter in view of a noise margin since Poon teaches that device noise margin varies across device samples due to process variations and because of this, the range of the device noise margin must be taken into account in setting up circuit rules and careful attention must be paid to all aspects of noise analysis to maintain system reliability (page 64).

Conclusion

55. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

56. Patra et al (US Patent Application Publication 2003/0066037) teaches determining a set of objective parameters for a circuit and receiving noise constraints for the circuit wherein values of the objective parameters are optimized based on the noise constraints.

57. Conn et al (US Patent 5,999,714) teaches a method of incorporating noise considerations during circuit optimization.

58. Wu et al (US Patent 6,826,736) techniques for considering whether the effects of cross-talk coupling and other noise exceed the noise tolerance of a circuit.

59. Cernea (US Patent 7,046,568) teaches a sensing module that operates with a sense amplifier sensing a conduction current of a memory cell via a coupled bit line under constant voltage condition in order to minimize bit-line to bit-line coupling.

60. Taylor (US Patent 5,978,293) teaches techniques that allow for the construction and operation of dynamic SRAM sense amplifiers which substantially reduce or eliminate the DC power consumed by conventional SRAM sense amplifiers, reduce the AC power consumed by the output drivers, and substantially reduce the output switching noise.

61. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C. Jacob whose telephone number is 571-272-6249. The examiner can normally be reached on M-F 7AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Mary C. Jacob
Examiner
AU2123

MCJ
11/9/06

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PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100